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Fig. 23 shows a cross section view of a sixth embodiment of the invention.

Fig. 24 shows a cross section view of a seventh embodiment of the invention.

Fig. 25 shows a cross section view of an eighth embodiment of the invention.--.

Page 8, line 17, change "4" to --5--.

Page 8, line 23, change "sacrificiaal" to --sacrificial--.

Page 9, line 9, change "oxide" to --dielectric--.

B2 Page 9, line 11, change "Gate oxide 26 may" to --Gate dielectric 26 may be, for example, silicon oxide, silicon nitride, silicon oxynitride, or a silicon oxide/silicon nitride composite, and may--.

Page 9, line 12, after "20" insert --nm--.

Page 9, line 16, change "oxide" to --dielectric--.

Page 9, line 18, change "sacrificial" to --insulating--; same line, change "14" to --18--; same line, change "oxide" to --dielectric--.

Page 9, line 21, change "oxide", second occurrence, to --dielectric--.

Page 10, line 2, change "co planar" to --coplanar--.

Page 11, line 9, change "atoms/cm3" to --atoms/cm^3--.

Page 11, line 18, change "oxide" to --dielectric--.

Page 11, line 22, change "oxide" to --dielectric--.

Page 12, line 1, change "oxide" to --dielectric--.

Page 12, line 7, change "titanium or platinum" to --Al, Er, Hf, Nb, Pt, Ta, Ti, Y, W or Zr--.

Page 12, after line 15, insert two new paragraphs --The oxidation process for oxidizing metal layer 16 in gate window 19 to form gate dielectric 50 may be thermal. In this case, insulating layer 18 must also act as a diffusion barrier to oxygen to prevent oxidation of the source/drain metallurgy, metal layer 16 beneath insulating layer 18. A preferred material for insulating layer 18 would be silicon nitride. SiO_2 is not as preferred as a material since it is typically too permeable to ambient oxygen during oxidation.

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Gate dielectric 50 may alternatively be formed by an electrochemical anodic oxidation process, such as described in Handbook of Thin film Technology, by Maissel and R. Glang, McGraw Hill (1983), chapters 5 and 19. Electrochemical anodic oxidation of metal layer 16 in gate window 19 may be used to produce metal oxides which may be for example Al_2O_3, Er_2O_3, HfO_2, Nb_2O_5, PdO, PtO, Ta_2O_5, TiO_2, WO_3, Y_2O_3 and ZrO_2 from respective metals Al, Er, Hf, Nb, Pd, Pt, Ta, Ti, W, Y and Zr. Some of the above metals may form oxides other than those listed above. Furthermore, some of the above mentioned metal oxides such as PdO and PtO may be less preferred due to their relatively high conductivities. The other oxides listed above are preferred. Relative to thermal oxidation, electrochemical anodic oxidation processes have the advantages of (i) lower processing temperature in the range where the electrolyte is in the liquid phase, typically from about 0°C to about 100°C, (ii) greater spatial selectivity, in that oxidation will only begin on metal surfaces directly in contact with the electrolyte, and (iii) easier process control over uniformity and endpoint. For example, control over process uniformity may be easier because the maximum metal oxide film thickness can be set by the applied voltage, instead of by the time integral of an average current density that may show strong local variations. This self-limiting aspect of oxide formation thus makes it easier to make a uniform oxide over a wider variety of pattern densities and feature sizes. Additional process parameters influencing oxide quality and

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thickness include the metal type and purity, and the electrolyte composition and temperature.

Gate dielectric 50 may alternatively be formed in gate window 19 by a reaction of metal layer 16 and a gaseous plasma to produce an oxide, nitride or oxynitride. Formation of gate dielectric 50 by the process of electrochemical anodic oxidation, plasma oxidation or plasma nitridation may further include one or more subsequent thermal treatments, for example, heating in a reactive or nonreactive ambient to a temperature above a selected temperature.--.

Page 13, line 4, delete "or on gate dielectric 26".

B4 Page 13, line 14, after "." insert two new sentences, --After formation of epitaxial channel layer 52, a gate dielectric 26 is formed over channel layer 52, the sidewalls of gate window 19, and on the upper surface of insulating layer 18. A T-shaped gate 32 of gate material 30 is formed over gate dielectric 26.--.

Page 14, line 8, change "oxide" to --dielectric--.

Page 14, after line 25, insert several new paragraphs, --A schematic of an electrochemical anodic oxidation set-up to form the structure of Fig. 15 is shown in Fig. 21. The electrochemical cell consists of housing 63 containing electrolyte solution 64, a working piece such as metal layer 16 acting as electrode 67, and counter electrode 68 positioned in electrolyte solution 64 spaced from metal layer 16. Electrolyte solution 64 may be for example concentrated HNO_3, 0.1% to 10% citric acid, or about 10% acetic acid. Insulating layer 18 protects underlying metal layer 16 of regions that will become the source/drain 74 metallurgy.

Fig. 22 illustrates a top view of several gate oxide regions 50 in respective gate windows 19 surrounded by insulating layer 18 and still-connected metal layer 16 below insulating layer 18 which will be subsequently patterned to form source/drain 74 contact regions on either side of gate oxide 50. Metal layer 16 on substrate 1 may be used as the electrode throughout the anodization process since the gate oxide regions 50 in respective gate windows 19 are always formed as isolated islands that do not interfere with the connectedness of the surrounding source/drain 74 electrode metal.

T-shaped gate structures incorporating a gate oxide or nitride formed by oxidation or nitridation of an in-situ metal layer 16 need not be limited to the device geometry shown in Fig. 16. For

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example, the source/drain metallurgy may consist of a bottom metal layer 16 which is locally oxidized or nitridized in gate window 19 to form gate dielectric 50. One or more conductive layers of low resistance material may be formed over metal layer 16 to reduce the source/drain resistance.

Fig. 23 shows an embodiment of a field effect transistor 76 containing a double layer source/drain metallurgy comprising bottom layer 16 and top layer 78. Gate dielectric 50 is a metal oxide, nitride, or oxynitride of the metal used for bottom layer 16. Insulating sidewall layers 79 in the gate window may be formed on the sidewalls of top layer 78 before, during or after formation of gate oxide 50, by a process such as thermal oxidation, electrochemical anodic oxidation, plasma oxidation, plasma nitridation, or combinations thereof, to electrically isolate layer 78 from subsequently formed T-shaped gate 32. A second layer of low resistance material 80 may be formed over gate material 30 prior to patterning to form T-shaped gate 32.

The embodiment in Fig. 23 has the advantage that upper conductive material 78 may be selected for its low resistivity while bottom conductive material 16 may be selected for the electrical qualities of its oxide or nitride dielectric, its Schottky barrier properties, and its compatibility with the underlying substrate material 1. Metal layer 16 should preferably be thin to enable complete oxidation of metal layer 16 with a minimum of oxidation

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B5 under layer 78 at the edges of gate window 19, to avoid increasing the gate length of transistor 76.

An alternative to the insulating sidewall layers 79 is shown in Fig. 24, where field effect transistor 82 contains a double layer source/drain metallurgy comprising bottom layer 16 and top layer 78. As in Fig. 23, gate dielectric 50 is a metal oxide, nitride, or oxynitride of the metal used for bottom layer 16. Insulating sidewall spacers 84 are formed by conformally depositing a thin dielectric layer on metal layer 16 in gate window 19, sidewalls of conductive material 78 in gate window 19, and upper surface of insulating layer 18, and then anisotropically etching said thin dielectric layer by a process such as reactive ion etching (RIE) to produce sidewall spacers 84. Metal layer 16 in the gate window 19 may also be etched to reduce thickness and to clean the surface prior to oxidation or nitridation.

The bottom metal layer 16 should ideally not react with or consume the underlying semiconductor substrate 1, and should act as a barrier against the reaction of the upper conductive layer 78 with substrate 1. An example of a suitable bottom layer 16/top layer 78 combination is Ta/Al. Ta is a good barrier material and forms an excellent Ta_2O_5 gate oxide. However, the resistivity of Ta in its thin film beta phase form is 170 micro-ohm-cm which is too high for it to be used alone as a source/drain contact metal. In contrast,

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Al has a low resistivity. However, without a material such as Ta to act as a barrier to such reaction, the Al may react with substrate material 1 during anneals required in subsequent process steps in forming an integrated circuit.

Fig. 25 shows another field effect transistor structure 88 having the same double layer source/drain metallurgy as the structures 76 and 82 in Figs. 23 and 24. Dielectric 90 replaces gate dielectric 50 and sidewall insulators 79 or 84 shown in Fig. 24, and is deposited in gate window 19, on the sidewalls of conductive material 78 in gate window 19, and on upper surface of insulating layer 18. Dielectric 90 may be a deposited silicon oxide, silicon nitride, or silicon oxynitride, or silicon oxide/silicon nitride composite or it may be an oxide, nitride, or oxynitride of a deposited metal layer, formed for example by deposition of Al, Er, Hf, Nb, Ta, Ti, W, Y, Zr and mixtures thereof and subsequent electrochemical anodic oxidation, thermal oxidation, gaseous plasma anodization, or combinations thereof.--.